REMARKS

Claims 1-20 are rejected in the application. Claims 1, 3, 4, 10, 11, 13, 14 and 20 have been amended. Claims 2 and 12 have been cancelled, and claims 1, 3-11, and 13-20 remain in the application. It is respectfully submitted that no new matter has been added.

Claim Rejections under 35 U.S.C. § 103

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nizar et al., U.S. Patent No. 5,495,615 (hereinafter "Nizar"). In response to Applicants' argument that Nizar does not teach or suggest a method and apparatus to establish thread priority in a *single* processor, the examiner "points out that a typical processor in the database art, including Nizar, is in fact a logical multiple processing entities in unison." Although the examiner admits "the distinction between single and multiple processing units is a blurry one," the examiner took official notice that using a single processor instead of multiple processors is well known and equivalent. Applicants respectfully submit that there is a distinction that can be made, particularly when applied to the invention of Nizar as against the invention disclosed by Applicants.

The examiner fails to acknowledge the thrust of Applicants' argument based on the amendments from the Office Action response dated August 7, 2002. Applicants respectfully submit that the multiple processor interrupt controller (MPIC) of Nizar is inherently different than the method and apparatus of establishing thread priority for a number of resources in a processor as described by Applicants. For each *single* processor, a wide variety of resources are disclosed by Applicants, each which may utilize the method of establishing thread priority. The execution and priority of each thread may be parsed for each resource unit within the execution

pipeline of a single processor. Applicants have disclosed that each of these resources may utilize the method of establishing a priority, which include, but are not limited to, the decode unit, trace cache / MSROM unit, rename unit, out of order execution unit, and retire unit (see Applicants' Detailed Description, pg. 5, para. 1).

Nizar, on the other hand, teaches a method and apparatus to prioritize multiple processors within and between multiple clusters of processors. Nizar only discloses these two basic modes of operation for utilizing processor priority, referred to as operating in "intra-cluster" or "inter-cluster" systems (col. 11, l. 64 to col. 12, l. 60). Nizar neither discloses nor suggests an apparatus or method to establish thread priority within the individual resources or sub-units within a processor. Applicants have amended independent claims 1, 10, 11, and 20, to include the individual resources allocated for the plurality of threads to further bring out this feature of the invention. Applicants' specification and claims support and disclose the individual resources within a single processor. No new matter has been added.

As to claim 11, the examiner cites to several passages in Nizar. In one particular passage, col. 4, ll. 51-67, Nizar discusses programmable interrupt controllers (PIC) in uniprocessor systems and the ability to assign a priority to each interrupt request line. However, Nizar neither teaches nor suggests the method and apparatus of establishing thread priority for a resource in a single processor, as disclosed by Applicants. Within the same passage cited by the Examiner, Nizar distinguishes between the solutions to issues as they pertain to interrupt controller computer architecture in a uniprocessor (i.e. single processor) system versus those in a multiprocessor environment. Even here, Nizar identifies that the solutions for designing a PIC are different and makes a clear distinction concerning inventions utilized in a single processor (prior art described by Nizar) and that utilized in a multiprocessor system (the invention of

Nizar). Thereby, Applicants submit that, likewise, for a method and apparatus for establishing thread priority for a resource, the solution is distinct between that found for a single processor and another for multiple processors. Based on the foregoing arguments and amendments, Applicants respectfully submit that claim 11 is allowable

As to claims 12-19, examiner states that Nizar disclosed a resource allocated between the plurality of threads depending on a priority assigned to each thread, wherein the resource is a decode unit in a processor system, citing col. 12, ll. 43-60. Applicants respectfully submit that the examiner has misinterpreted the passage as disclosing Applicants' invention. While Nizar does disclose a resource allocated between the plurality of threads depending on a priority assigned, the "resource" to be allocated is explicitly defined by Nizar as each one of the processors in a multiprocessor system. As Nizar explains, "[e]ach processor has a processor priority that reflects the relative importance of the code the processor is currently executing." (col. 12, ll. 52-52). Only in passing does Nizar refer to the queue and decode units, that "the sender cluster sends a message in logical destination mode over its I-Bus. Cluster Manager 600 accepts the message, puts it in the Receive Logic Unit 603 receive queue and decodes the address information to determine the destination cluster." (col. 12, ll. 41-45).

From the quoted passage, Nizar clearly does *not* disclose that a thread priority is established and queued for the decode unit itself. Rather, the interrupt messages are sent through queues and decode units for establishing processor priority solely in a multiprocessor environment. Therefore, Applicant respectfully submits that Nizar fails to teach or suggest that a resource, such as a decode unit, is allocated between a plurality of threads depending on the priority assigned to each thread. Dependent claims 2 and 12 have been cancelled to include this feature as a limitation in independent claims 1 and 11. This feature that includes a resource

allocated between a plurality of threads in a single processor has also been added to amended independent claims 10 and 20. In addition, Applicants respectfully submit that claims 13-19 are allowable as depending from an allowable base claim 11.

As to claim 20, the features discussed above for independent claim 11 have been added to claim 20 to more clearly define the invention. Applicant submits, therefore that claim 20 is allowable based on the arguments set forth above.

As to claims 1-10, the method claims are deemed to be made inherent by the functions of the apparatus structure of claims 11-20, and were rejected for the same reasons. As previously noted, claims 1 and 10 have been rewritten and resemble the apparatus structure of claims 11 and 20, respectively. Therefore, the foregoing arguments addressing the examiner's rejections should be applied to claims 1-10.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 1-20 under 35 U.S.C. § 103(a) is respectfully request

CONCLUSION

For all the above reasons, the Applicants respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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Dated: JuLY 24, 2003 By: _____

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